

DEVICE PARAMETERS 1/

JPL PART #	MFR	GENERIC PART NO.	RADIATION LEVEL (TID) (RAD(S)) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CONNECTION TABLE
12158-E01060FR	HONEYWELL SSEC	HR1060 - RSDL	100K	FIG. 5-3 HEREIN (256-LEAD FLATPACK)	FIG. 5-1 HEREIN	TABLE 4-4 & 4-5 HEREIN	TABLE 4-1 HEREIN	TABLE 4-7 HEREIN

NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515837B AND MIL-I-38535, LEVEL V, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.
 2/ THE POST-IRRADIATION PARAMETRIC LIMITS SHALL BE THOSE OF TABLES 4-4 & 4-5 HEREIN.
 3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

RELEASED THRU SECTION 356 DATA MANAGEMENT:			DATE:	
REVISION: C APPROVED BY (Section 507): APPROVED BY (Section 341):			DATE: DATE:	
APPROVED SOURCE(S)				
VENDOR PART NO.	VENDOR		JPL PART NO.	
22016910	HONEYWELL INC. SOLID STATE ELECTRONIC CENTER PLYMOUTH, MN 55441 CAGE NO. 34168		12158 - E01060FR	
JET PROPULSION LABORATORY CALIFORNIA INSTITUTE OF TECHNOLOGY			CAGE NO. 23835	
Procurement Specification: CS515837	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, REED SOLOMON DOWN LINK (RSDL)			DETAILED SPECIFICATION
Screening Specification: CS515837, ST12158				ST 12158
Custodian: Parts Reliability Group Section 514				SHEET 1 OF 32

CHANGE INCORPORATION LOG

CHG LTR	ENGINEERING APPROVAL			PAGES AFFECTED	RELEASED THRU		
	INITIAL	SECTION	DATE		INITIAL	SECTION	DATE
A	HS	514	9/7/93	Initial Release	NH	356	9/8/93
	SW	348	9/7/93				
B	HS	514	10/11/93	5, 7, 9, 10, 18, 21, 26, 27, 29, 32	RA	356	10/22/93
	SW	348	10/11/93				
C	HS	507	12/22/94	19, 22, 29			
	SW	341	12/22/94				

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Scope

This is the detailed specification for a space-qualified *Reed-Solomon Downlink* gate array for the Command Data Subsystem. This document shall be the sole source of design specifications for the RSDL gate array, and shall supersede any other specification documents issued prior to this release.

Applicable Documents

- o *General Specification for Gate Array Application Specific Integrated Circuits (ASICs), 24 March 1992, CS515837, Rev. B*

This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.

- o *Reed-Solomon Downlink Bus Arbiter Timing Unit, Functional Specification, Version 2.0, February 9, 1993.*

This document is the primary source of the functional specifications of the space qualified Reed-Solomon Downlink (RSDL) ASIC device for the CASSINI Mission.

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1. CHIP OVERVIEW

The Reed-Solomon Downlink (RSDL) gate array is used in the Command and Data Subsystem (CDS) on the Cassini spacecraft. A block diagram of the RSDL gate array is shown below. The RSDL gate array consists of three functional blocks: the RSDL block, the Timing Unit (TU) block, and the Bus Arbiter (BA) block. The primary function of the RSDL block is format telemetry data and send it to the Radio Frequency Subsystem (RFS). The Timing Unit generates various timing signals used within CDS. It also maintains spacecraft time. The Bus Arbiter performs the arbitration function on the multi-master ISB bus.

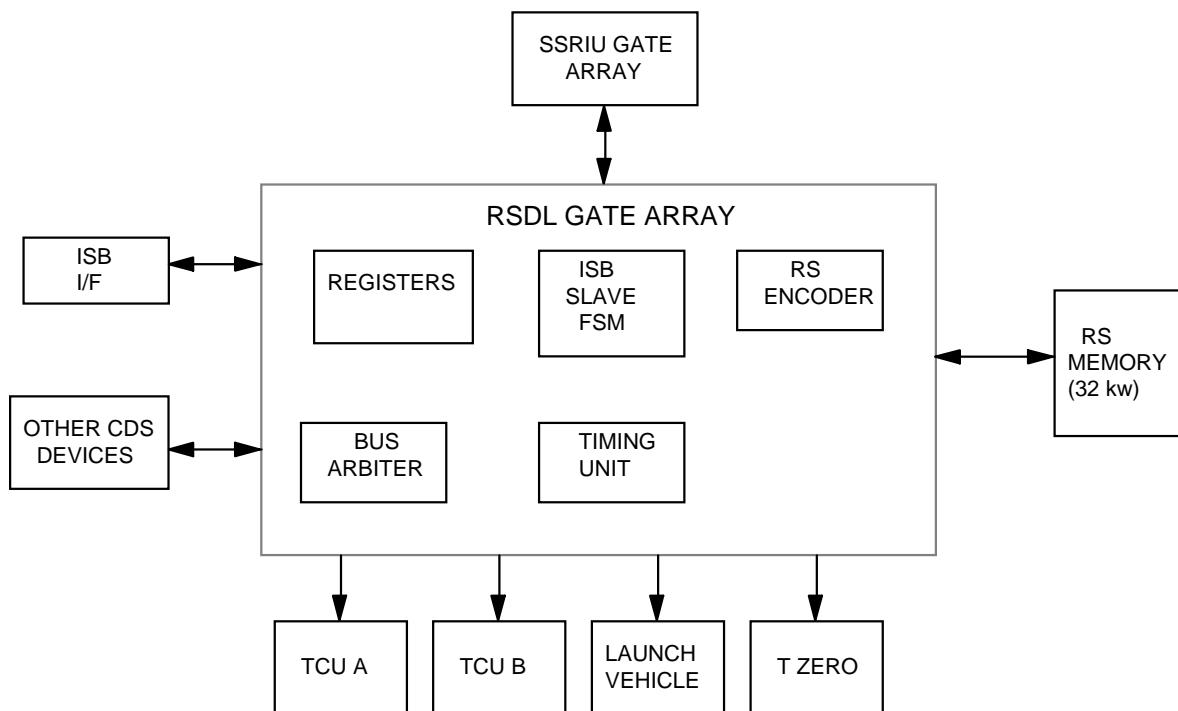


Figure 1-1. RSDL Functional Block Diagram

2. RSDL ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS

2.1 RSDL ASIC Symbol

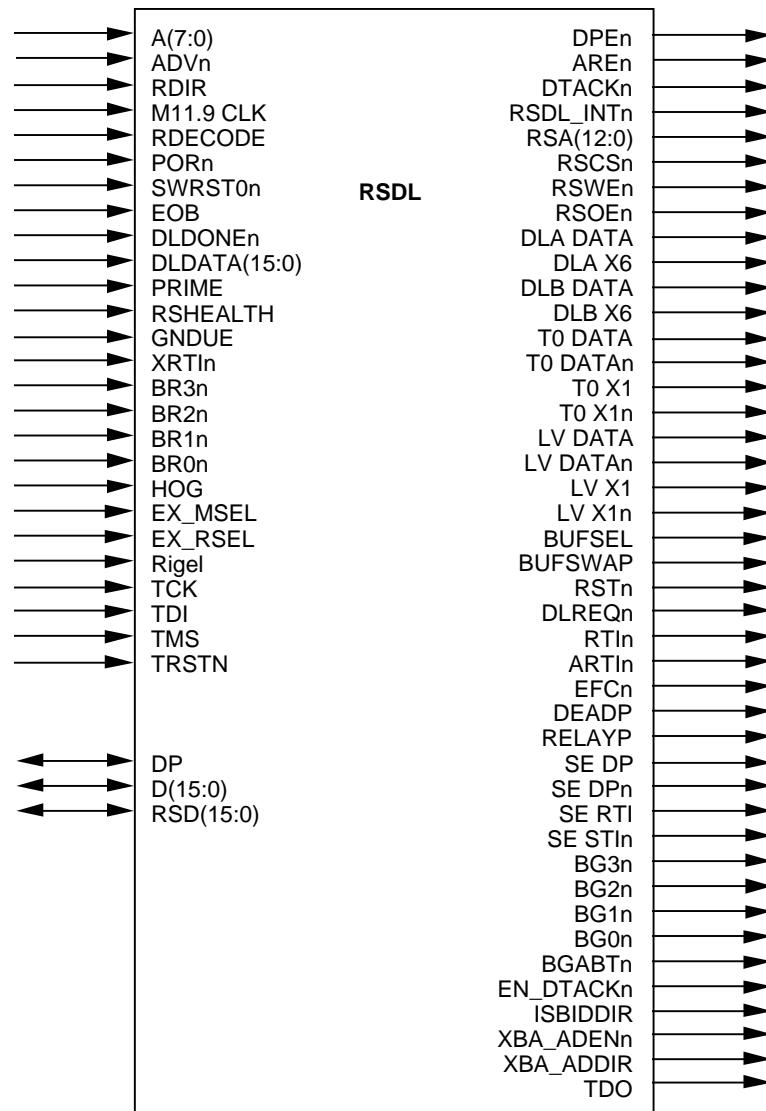


Figure 2-1. RSDL ASIC Symbol

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2.2 Signal Description

Name	Pin No. ¹	Type ²	Description
A(7:0)	174-176, 185-187, 189, 190	IN	ISB Address Bus (256W).
DP	120	BI6	ISB Data Parity.
D(15:0)	124, 126, 132, 134, 136, 138, 140, 145, 147, 151, 153, 155, 159, 161, 163, 165	BI6	ISB Data Bus.
DPEn	143	OUT6	ISB Data Parity Error. It indicates that illegal ISB data parity has been detected during the current ISB write cycle.
AREN	122	OUT6	ISB Address Range Error. It indicates that ISB is accessing an undefined register.
ADVn	118	IN	ISB Address Valid.
RDIR	114	IN	ISB Read Direction. It indicates an ISB read cycle when it is high, an ISB write cycle when it is low.
DTACKn	105	OUT6	ISB Data Transfer Acknowledge. It indicates the data transfer is complete.
RSDL_INTn	116	OUT6	RSDL Interrupt line. It is asserted when an internal error has been detected. The cause of the interrupt can be seen in the Interrupt Register.
M11.9_CLK	77	INPD	11.9448MHZ clock comes from the crystal.
RDECODE	84	IN	Select Local Register. ISB accesses RSDL internal register. This decoded line comes from the HCD/CRC device.
PORn	73	IN	Power On Reset. This signal comes from HCD/CRC.
SWRST0n	80	IN	Software Reset 0. This signal comes from HCD/CRC.
RSA(12:0)	14, 16, 26, 27, 29, 31, 32, 35, 36, 38, 40, 41, 48	OUT6	RS Memory Buffer Address Bus.
RSD(15:0)	4, 6, 8, 11, 13, 18, 20, 24, 50, 53, 55, 58, 60, 62, 69, 71	BI6	RS Memory Buffer Data Bus.

Table 2-1. Signal Descriptions

¹ The pin numbers of bus signals are in the same sequence as the signals.

² For a description of the signal type refer to Table 4-9.

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Name	Pin No. ³	Type ⁴	Description
RSCSn	33	OUT6	RS Memory Buffer Chip Select.
RSWEn	46	OUT6	RS Memory Buffer Write Enable.
RSOEn	43	OUT6	RS Memory Buffer Output Enable.
DLA_DATA	240	OUT6	Downlink Data to TCU A.
DLA_X6	239	OUT6	Six times Downlink Data Rate Clock to TCU A.
DLB_DATA	237	OUT6	Downlink Data to TCU B.
DLB_X6	236	OUT6	Six times Downlink Data Rate Clock to TCU B.
T0_DATA	234	TRIOD6	Downlink Data to T0.
T0_DATAn	233	TRIOD6	Downlink Data in reverse polarity to T0.
T0_X1	231	TRIOD6	Downlink Data Rate Clock to T0.
T0_X1n	230	TRIOD6	Downlink Data Rate Clock in reverse polarity to T0.
LV_DATA	245	OUT6	Downlink Data to LV.
LV_DATAn	246	OUT6	Downlink Data in reverse polarity to LV.
LV_X1	243	OUT6	Downlink Data Rate Clock to LV.
LV_X1n	242	OUT6	Downlink Data Rate Clock in reverse polarity to LV.
BUFSEL	173	OUT6	Buffer Select for the DL buffer. 0 selects the A buffer, 1 selects the B buffer. This signal goes to the SSRIU device.
BUFSWAP	183	OUT6	Swap the DL buffer. This signal goes to the SSRIU device.
EOB	167	IN	End of the DL buffer. This signal comes from the SSRIU device. It indicates that the end of the DL buffer has been reached.
RSTn	171	OUT6	Synchronous Reset. This is the combined Hardware/Software reset. This signal goes to the SSRIU device.
DLREQn	168	OUT6	DL request for memory read. This signal goes to the SSRIU device.
DLDONEn	169	IN	DL request has been served. This signal comes from the SSRIU device.

Table 2-1. Signal Descriptions (Cont'd)

³ The pin numbers of bus signals are in the same sequence as the signals.

⁴ For a description of the signal type refer to Table 4-9.

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Name	Pin No. ⁵	Type ⁶	Description
DLDATA(15:0)	179-181, 196, 197, 199, 200, 202, 203, 205, 206, 208, 209, 211, 213, 214	IN	DL Data bus. This bus comes from the SSRIU device.
PRIME	100	IN	Prime indicates whether this CDS string is a primary string or not. This signal comes from the HCD/CRC chip.
RSHEALTH	101	IN	Redundant String Health. This signal comes from HCD/CRC chip
GNDUE	111	IN	Ground Update Enabled. It is used to indicate if the ground wants to update the S/C time. It is a CRC bit.
XRTIn	112	IN	Cross-strapped RTI. This signal comes from the XBA chip.
RTIn	103	OUT6	Real Time Interrupt. The pulse width is 1.004μs.
ARTIn	109	OUT6	ARTIn occurs 5ms before RTI. The pulse width is 1.004μs.
EFCn	90	OUT6	64.005 Hz clock with 1.004μs pulse width.
DEADP	96	OUT6	Dead Period. It is the time between the end of the ARTI and the beginning of the RTI.
RELAYP	98	OUT6	2048.148 Hz clock with 1.004μs pulse width.
SE_DP	228	TRIOD6	DEADP sent to SE.
SE_DPN	227	TRIOD6	DEADPn to SE.
SE_RTI	225	TRIOD6	RTI to SE.
SE_RTIn	224	TRIOD6	RTIn to SE.
BR3n	249	IN	ISB Bus Request 3. Signal from the XBA and the EFC.
BR2n	252	IN	ISB Bus Request 2. Signal from the XBA and the EFC.
BR1n	93	IN	ISB Bus Request 1. Signal from the XBA and the EFC.
BR0n	254	IN	ISB Bus Request 0. Signal from the XBA and the EFC.
BG3n	248	OUT6	ISB Bus Grant 3. Signals to the XBA and the EFC.
BG2n	250	OUT6	ISB Bus Grant 2. Signals to the XBA and the EFC.
BG1n	92	OUT6	ISB Bus Grant 1. Signals to the XBA and the EFC.
BG0n	253	OUT6	ISB Bus Grant 0. Signals to the XBA and the EFC.
BGABTn	115	OUT6	Bus Grant Abort.
HOG	94	IN	The HOG signal forces the Bus Arbiter to only grant the ISB bus to the XBA and the EFC.

Table 2-1. Signal Descriptions (Cont'd)

⁵ The pin numbers of bus signals are in the same sequence as the signals.

⁶ For a description of the signal type refer to Table 4-9.

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Name	Pin No. ⁷	Type ⁸	Description
EX_MSEL	82	IN	External Memory Select. This is the MDECODE of the SSRIU chip. It indicates the SSR/DL memory of the SSRIU being accessed.
EX_RSEL	83	IN	External Register Select. This is the RDECODE of the SSRIU chip. It indicates an internal register of the SSRIU being accessed.
EN_DTACKn	107	OUT6	Enable DTACKn. This will enable 2A1 DTACKn signal.
ISB1DDIR	75	OUT6	ISB Data Bus Direction for 2A1 Board. This signal controls 2A1 ISB Data bus directions. It is a delay version of RDIR.
XBA_ADENn	86	OUT6	XBA Address Enable. This signal will enable 2A2 board Address bus when XBA is the bus master.
XBA_ADDIR	88	OUT6	XBA Address bus Direction. This signal will control 2A2 board Address bus direction.
Rigel ⁹	220	INPD	Rigel test command. Forces internal logic to assume functionality compatible with the Rigel test vector generation tool.
TCK ⁹	217	INPD	Test Circuitry Clock.
TDI ⁹	221	INPU	Test Data In. Serial data in for scan path test logic.
TMS ⁹	222	INPU	Test Mode Select. Commands the scan logic mode.
TRSTN ⁹	216	INPU	Test Reset. Forces all nodes visible to the scan paths to a known state for test purposes; not necessarily the same state values as nPOR.
TDO ⁹	218	TRI6	Test Output Data. Serial bit stream from the internal scan paths.
PWR	1, 65, 129, 193	VDD	Vdd Power Pads.
GND	2, 63, 64, 66, 127, 128, 130, 191, 192, 194, 255, 256	VSS	Vss Power Pads.

Table 2-1. Signal Descriptions (Cont'd)

⁷ The pin numbers of bus signals are in the same sequence as the signals.

⁸ For a description of the signal type refer to Table 4-9.

⁹ These signals are defined for use with the Honeywell On-Chip Monitor (OCM) scan path control block, and their Rigel test vector generator. See Honeywell manuals for precise definitions of these signals. These signals are not used in flight hardware.

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3. FUNCTIONAL DESCRIPTION

3.1 RSDL Functional Block

The RSDL block performs the following functions:

- (1) The RSDL supports the CCSDS Packet Telemetry protocol. The RSDL reads in Transfer Frames from the SSRIU and forms Downlink Frames which meet the CCSDS standard. The Downlink Frames are then sent to RFS. A Downlink Frame is composed of three fields, each field is described below.

Sync Pattern:

The Sync Pattern consists of 32 bits and has the value 1ACF FC1D hex. The Sync Pattern is used on the ground to determine the start of each Downlink Frame.

Transfer Frame:

The engineering and science data that needs to be sent to the ground is found in the Transfer Frame. The Transfer Frame consists of the Source Packets which are composed in the various science and engineering subsystems, or in CDS. While the RSDL allows the size of the Transfer Frame to vary, currently there are plans to use only one size during the mission, 8800 bits.

Reed-Solomon (RS) Check Bits:

These check bits provide error detection and correction on the Transfer Frame only; the check bits do not cover the Sync Pattern. The encoder is based on a design by E. R. Berlekamp. The code used is defined as a (255,223) code with an interleaved depth of 5. The RSDL allows RS encoding to be turned on and off. The RS check are stored in the RS memory buffer, which consists of two 32kx8 IBM SRAMs.

SYNC PATTERN (32 bits)	TRANSFER FRAME (8800 bits)	REED-SOLOMON CHECK BITS (1280 bits)
------------------------------	-------------------------------	---

DOWLINK FRAME (10,112 bits)

- (2) The RSDL reads downlink data from the SSRIU gate array. The RSDL retrieves data from one of two buffers in the SSRIU. A Downlink Frame is composed as follows: at the start of a Downlink Frame, the RSDL chip first sends the Sync Pattern to RFS. It then reads the Transfer Frame from the SSRIU and passes it on to RFS. As the Transfer Frame passes through the RSDL chip, it calculates the RS check bits and accumulates them in the RS memory buffer. At the end of the Transfer Frame, the RSDL chip sends the RS check bits to RFS.

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The SSRIU contains two DL Buffers. At any point in time one is active, meaning the RSDL is reading Transfer Frames from this buffer. The other buffer is inactive, allowing software to load it with Transfer Frames. This process is illustrated below.

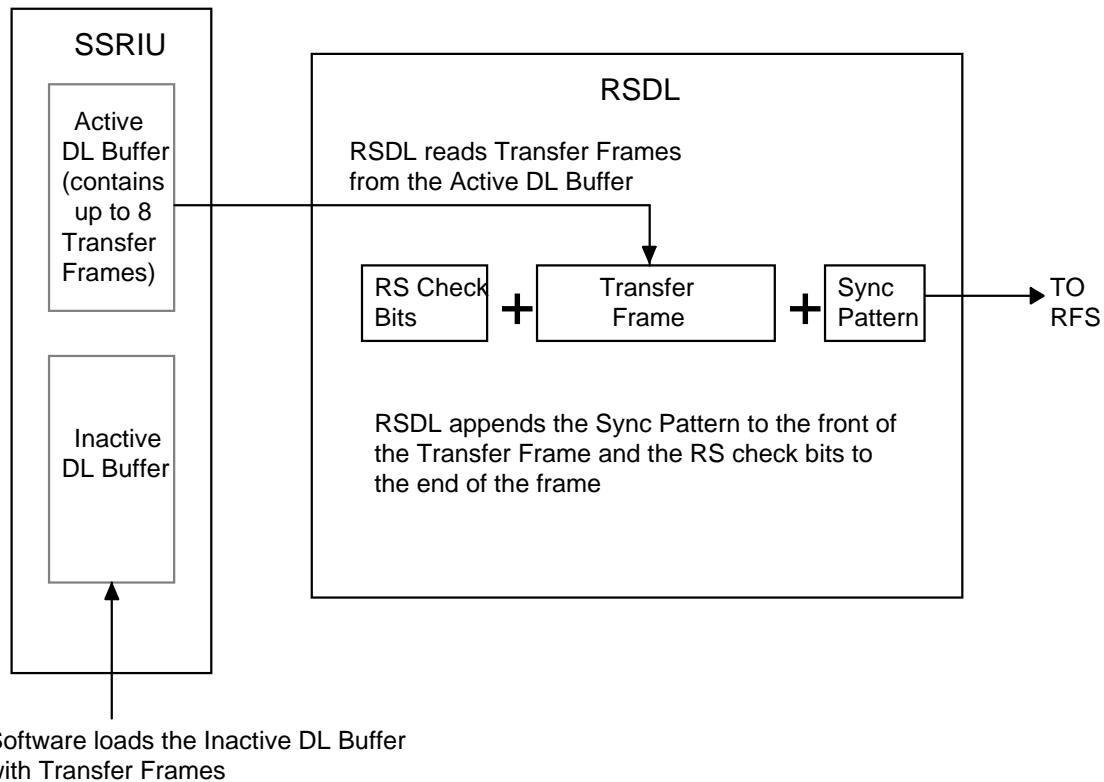


Figure 3-1. RSDL Transfer Frames

- (3) The RSDL supports a variable downlink rate ranging from 5 bits per second (bps) to 248,850 bps. A clock that is six times the data rate is sent to RFS. The downlink data changes on the falling edge of this clock.
- (4) Downlink data and the data rate clock are also sent to the T-Zero interface. On this interface the downlink data changes on the rising edge of the clock.
- (5) The downlink data and data rate clock are also sent to the Launch Vehicle interface. All of the signals on this interface have a pulse width of 334 ns. The clock rate is the same as the data rate.
- (6) The RSDL allows spacecraft time to be correlated with a specific bit in a downlink frame.

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3.2 Timing Unit (TU) Functional Block

The TU performs the following functions:

- (1) The TU provides the following timing signals to the rest of CDS:

RTI: The RTI (Real Time Interrupt) signal used by the software to schedule tasks; it is asserted 8 times per second.

ARTI: This signal occurs 5 ms. before RTI. It is an interrupt to the software; it marks the start of the dead period on the 1553 spacecraft bus.

EFCn: This 64 Hz interrupt allows software to schedule tasks with sub-RTI timing.

DEADP: This signal is asserted during the 5 ms. dead period. When asserted, it prevents the drivers for the 1553 spacecraft bus from driving the bus.

RELAYP: This 2 kHz clock is used by the relay driver to toggle the relays.

- (2) The TU contains a 46 bit counter which is used to maintain spacecraft time. The lower 14 bits maintain sub-second time; the upper 32 bits count elapsed seconds. The resolution of the counter is 61 us.; its maximum count is 136 years. Software can read all 46 bits of spacecraft time. Software can load only the 32 upper bits of spacecraft time; whenever the upper 32 bits are loaded, the lower 14 bits are automatically cleared.

3.3 Bus Arbiter (BA) Functional Block

3.3.1 Overview

The Inter-Subassembly-Bus (ISB) is a 16 bit, multi-master, parallel bus used for communication between devices within the CDS, as shown below. When a device with master capability requires the ISB, it issues a Bus Request to the BA. Using the protocol described below, the BA eventually issues a Bus Grant to the device requesting mastership. Upon receipt of Bus Grant, the device starts transferring data over the bus. If the BA needs to take the bus away from a master before it is done using it, the BA will issue Bus Grant Abort. Upon receipt of Bus Grant Abort, the master may complete up to four more cycles, but must then give up the bus. A master gives up the bus by placing all of its bus drivers into tristate and then negating Bus Request.

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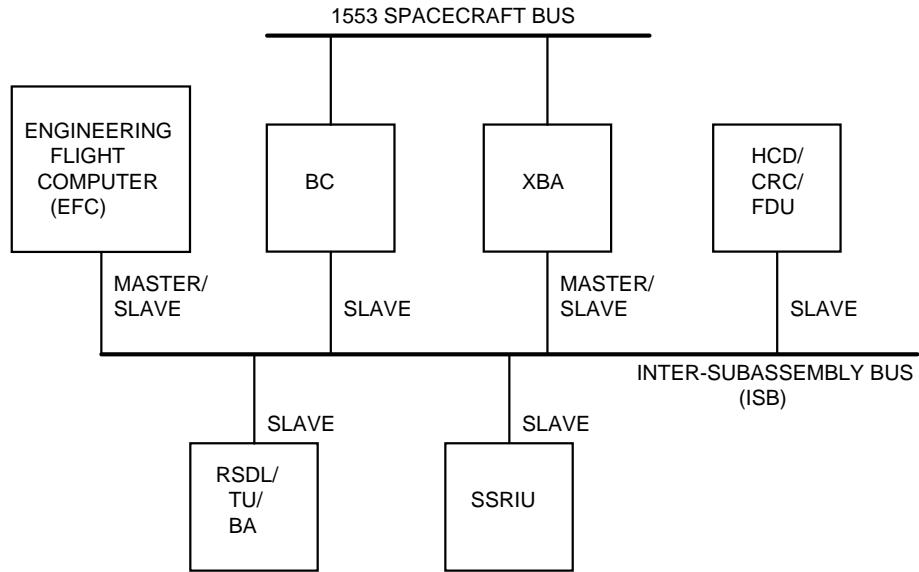


Figure 3-2. Inter-Subassembly-Bus (ISB)

3.3.2 Bus Allocation Policy

If a device has mastership of the ISB, and a second device asserts Bus Request, Bus Grant Abort is immediately asserted by the BA, independent of the priority of the two devices.

If two devices both assert Bus Request, when the bus becomes available, the higher priority device gets the bus, regardless of the order in which the Bus Requests were asserted. Priority is assigned as follows:

- Bus Request 0 (EFC) (highest priority)
- Bus Request 1 (XBA)*
- Bus Request 2 (unused)
- Bus Request 3 (unused) (lowest priority)

*When the HOG signal is asserted by the SE via the XBA, the XBA is the only device that gets the bus. Even when the XBA is not using the bus, no other device is granted bus mastership.

3.3.3 Bus Deallocation Policy

Release of the bus varies from device to device:

EFC: Once the EFC gets the ISB, it keeps the bus until Bus Grant Abort is asserted. Even if the EFC is not using the bus, it keeps it so long as Bus Grant Abort is not asserted. When the EFC receives a Bus Grant Abort, it may complete up to four more bus cycles before releasing bus mastership.

XBA: When the XBA gets the bus, it performs only one transaction and then releases the bus. The XBA must rearbitrate the next time the bus is needed. Since the XBA needs to perform at most only a single ISB cycle every 20 us., it does not even receive the Bus Grant Abort signal.

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3.3.4 XBA Address Buffer Control

The BA also controls the XBA ISB address buffers. The signal XBA_ADEN_n from the BA enables/disables the address buffers. The signal XBA_ADDIR controls the direction of the buffers. When the XBA is ISB master, the XBA address buffers drive the ISB. When the XBA is not the ISB master, the address buffers are pointer inward so that the XBA can receive the address from the ISB. Due to noise considerations, the buffers are disabled when swapping the direction of the buffers.

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4. ELECTRICAL CHARACTERISTICS

4.1 Electrical Test Requirements

Test	Subgroups (Per MIL-STD-883, Method 5005, Table 1)
Initial (Pre Burn-In)	1,7
Interim (Post Static I Burn-In)	1*,7*
Delta Calculations*,**	
Interim (Post Static II Burn-In)	1*,7*
Delta Calculations*,**	
Final (Post Dynamic Burn-In)	1*,2,3,7*,8,9,10,11
Delta Calculations*,**	
Group A	1,2,3,7,8,9,10,11
Group C End Point electrical***	1,2,3,7,8,9,10,11
Delta Calculations**	

Table 4-1. Electrical Test Requirements

- * PDA applies to these subgroups
- ** Deltas shall be calculated relative to the initial electrical parameters. Delta limits of Table 4-8 herein shall apply.
- *** Group C Lifetest shall be performed using the dynamic burn-in configuration of Table 4-7 herein.

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4.2 Absolute Maximum Ratings^{10,11,12}

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	Supply Voltage	-0.5	7.0	V
V _{IN}	Input Voltage Range	GND - 0.5	V _{DD} + 0.5	V
I _{OUT}	DC Output Current (per Output)		50	mA
P _D	Max. Package Power Dissipation		4	W
T _{ST}	Storage Temperature Range	-65	150	°C
T _S	Lead Temperature (Soldering, 5s)		270	°C
T _J	Junction Temperature		175	°C
Θ _{JC}	Thermal Resistance, Junction to Case		4	°C/W
V _{ESD}	ESD Protection Voltage - Class 2 (MIL-STD-883, Method 3015)	2000		V

Table 4-2. Absolute Maximum Ratings

4.3 Recommended Operating Conditions^{12,13}

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	Supply Voltage	4.5	5.5	V
T _A	Ambient Temperature	-55	125	°C
f _{max}	Max. Operating Frequency		12	MHz
t _r , t _f	Input Rise Time, Input Fall Time		500	ns

Table 4-3. Recommended Operating Conditions.

¹⁰ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.

¹¹ Values are guaranteed but not tested.

¹² -55°C ≤ T_c ≤ 125°C except as noted.

¹³ Extended operation outside recommended limits may degrade performance and effect reliability.

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4.4 DC Characteristics

4.4.1 DC Electrical Performance Characteristics

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Input Threshold Voltage	V_{IH}	$V_{DD}=5.5V$	1,2,3		3.85	V
	V_{IL}	$V_{DD}=4.5V$	1,2,3	1.35		V
Input Leakage Current	I_{IH1}^{14}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	μA
	I_{IH2}^{15}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	μA
	I_{IH3}^{16}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	50	550	μA
	I_{IL1}^{14}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-10	10	μA
	I_{IL2}^{15}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-550	-50	μA
	I_{IL3}^{16}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-10	10	μA
Output Leakage Current (Tristate)	I_{OZH}	$V_{DD}=5.5V, V_O=VDD$	1,2,3	-10	10	μA
	I_{OZL}	$V_{DD}=5.5V, V_O=GND$	1,2,3	-10	10	μA
Output Voltage	V_{OH}	$V_{DD}=4.5V, I_{OH}=-6mA$	1,2,3	4.0		V
	V_{OL}	$V_{DD}=4.5V, I_{OL}=6mA$	1,2,3		0.5	V
Output Current	I_{OH}	$V_{DD}=4.5V, V_{OH}=4.0V$	1,2,3		-6	mA
	I_{OL}	$V_{DD}=4.5V, V_{OL}=0.5V$	1,2,3	6		mA
Standby Supply Current	I_{DDSB}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=0$ Hz	1,2,3		800	μA
Quiescent Current	I_{DDQ}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=0$ Hz	1		5	μA
Operating Current	I_{DDOP}^{17}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=12$ MHz	1,2,3		100	mA
Input Capacitance ¹⁸	C_{IN}				15	pF
Output Capacitance ^{18,19}	C_{OUT}				15	pF

Table 4-4. DC Performance Characteristics

¹⁴ All Inputs, except: TDI, TMS, TRSTN, TCK, Rigel, M11.9_CLK.

¹⁵ Inputs with Pull-Ups: TDI, TMS, TRSTN.

¹⁶ Inputs with Pull-Downs: Rigel, M11.9_CLK, TCK

¹⁷ This value is based on the supplied functional test vector set and the ANDO tester loading (85 pF) and may not be applicable to system operation.

¹⁸ Guaranteed but not tested.

¹⁹ Refers to internal capacitance.

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4.4.2 Estimated Power Dissipation.

$$P_{\text{Total}} = P_{\text{Internal}} + P_{\text{Outputs}} + P_{\text{Quiescent}} = 340.3 + 24.2 + 4.4 = 368.9 \text{ mW}$$

$$P_{\text{Internal}} = \frac{1}{2} * f_{\text{CLK}} * C_{\text{Lint}} * (V_{\text{DD}})^2 = 340.3 \text{ mW}$$

Where:

C_{Lint}	=	$S * \# \text{of Nets} * 0.75 \text{pf}$
S	=	0.25
$\# \text{of Nets}$	=	10,000
f_{CLK}	=	12 MHz
V_{DD}	=	5.5V

$$P_{\text{Outputs}} = \frac{1}{2} * f_{\text{CLK}} * C_{\text{Lout}} * (V_{\text{DD}})^2 + P_{\text{Crowbar}} = 22.0 + 2.2 = 24.2 \text{ mW}$$

Where:

C_{Lout}	=	$S * \# \text{of Output Pads} * 50 (25) \text{ pf}$
S	=	0.04
$\# \text{of Output Pads}$	=	33 @ 50 pF 55 @ 25 pF
f_{CLK}	=	12 MHz
V_{DD}	=	5.5V
P_{Crowbar}	=	10% of P_{Outputs}

$$P_{\text{Quiescent}} = V_{\text{DD}} * I_{\text{DDSB}} = 4.4 \text{ mW}$$

Where:

V_{DD}	=	5.5V
I_{DDSB}	=	800 μA

4.4.3 IDDQ Testing.

Quiescent Current (IDDQ) testing shall be accomplished by using the Stuck-at Fault test vectors generated with RIGEL, or a subset thereof, as determined by JPL. Measurements shall be taken at every vector, unless otherwise indicated, recorded and compared to the IDDQ limit. The following statistical values shall be provided: Minimum, Maximum, Mean, Standard Deviation. The IDDQ limits shall be established by JPL after characterization of Engineering Model parts which are fabricated from the same wafer lot as the flight parts.

4.4.4 Pulldown Resistors.

The internal pulldown resistor design option has been used on the following input pads:

TCK
Rigel
M11.9_CLK

It is recommended that the TCK and Rigel signals be tied low (logic 0) in the flight hardware.

4.4.5 Pullup Resistors.

The internal pullup resistor design option has been used on the following input pads:

TDI
TMS

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TRSTN

It is recommended that the TDI and TMS signals be tied high (logic 1) in the flight hardware. TRSTN must be held low during power-up and therefore is recommended to be tied low (logic 0).

4.4.6 Open Drain Outputs.

Following Tristate Outputs are configured as Open Drain outputs:

T0_DATA	SE_DP
T0_DATAn	SE_DPN
T0_X1	SE_RTI
T0_X1n	SE_RTIn

DC parameters V_{OH} and I_{OH} for these Open Drain outputs can be measured by utilizing the serial scan to set the Open Drain outputs to a High state during test.

4.5 AC Characteristics

4.5.1 AC Electrical Performance Characteristics

Parameter	Symbol	Test Condition $V_{IN}=V_{DD}$ or GND	Subgroup	Specification Limit		Tester Limit ^{20,21}		Unit
				Min	Max	Min	Max	
Functional Tests		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=12 \text{ MHz}$	7,8	pass		pass		
Propagation Delay:		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
M11.9_CLK to DTACKn	t_{PLH1} t_{PHL1}		9,10,11	6 6	40 39	6.0 6.0	38.4 37.0	ns ns
M11.9_CLK to RSTn	t_{PLH2} t_{PHL2}		9,10,11	6 6	41 42	6.0 6.0	39.4 40.0	ns ns
M11.9_CLK to D(15:0)	t_{PZH1} t_{PZL1}		9,10,11	11 11	59 58	11.0 11.0	54.9 53.0	ns ns
Setup Time:		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
RDECODE to M11.9_CLK	t_{SU1}		9,10,11		17		17.0	ns
Hold Time:		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
M11.9_CLK to RDECODE	t_{HD1}		9,10,11		4		4.0	ns

Table 4-5. AC Performance Characteristics

²⁰ Tester limits are shown from a test perspective (i.e., set-up time, hold time are shown as max. limits).

²¹ Tester limits do not include guardbanding for tester errors.

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SHEET 21			SHEET 21	

4.5.2 Timing Analysis.

Pre-layout and post-layout timing shall pass the QuickSim simulation of the vectors supplied to the contractor without setup/hold timing violations.

4.5.2.1 Pre-Layout Timing Margins.

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library shall be supplied by the contractor. Critical paths will be identified and margin calculated via Mentor or Honeywell software toolsets, or a combination thereof.

4.5.2.2 Post-Layout Timing Margins.

Post-layout analysis of the device shall show positive margin on internal critical paths over all operating conditions. The analysis will follow the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the contractor.

4.5.2.3 Tester Specification Limits.

Tester limits in Table 4-5 have been adjusted for modified output levels and for differences in output loading in the ANDO tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the ANDO tester environment. The level at which an output is considered to have switched has been changed from 50% of VDD to 1V for low to high transitions and VDD-0.5V for high to low transitions for the 3mA buffer and to 1V for low to high transitions and VDD-1V for high to low transitions for the higher drive buffers (6mA, 9mA, 12mA, 15mA).

$$t_{\text{SPEC}}(\text{Tester}) = t_{\text{SPEC}}(\text{System}) - (T_{\text{Offset_fixed}} + C_{\text{Load}} * \text{LoadingFactor})$$

Where:

$$\begin{aligned} C_{\text{Load}} (\text{ System Simulation}) &= 25 \text{ pF} - \text{DTACKN, RSTN} \\ &\quad 50 \text{ pF} - \text{D}(15:0) \end{aligned}$$

For 6 mA drive buffer:

Low to High transition:	$T_{\text{Offset_fixed}} = -1.0 \text{ ns}$	$\text{LoadingFactor} = 0.103$
High to Low transition:	$T_{\text{Offset_fixed}} = -1.0 \text{ ns}$	$\text{LoadingFactor} = 0.121$

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SHEET 22			SHEET 22

4.5.3 Tester Load Circuit

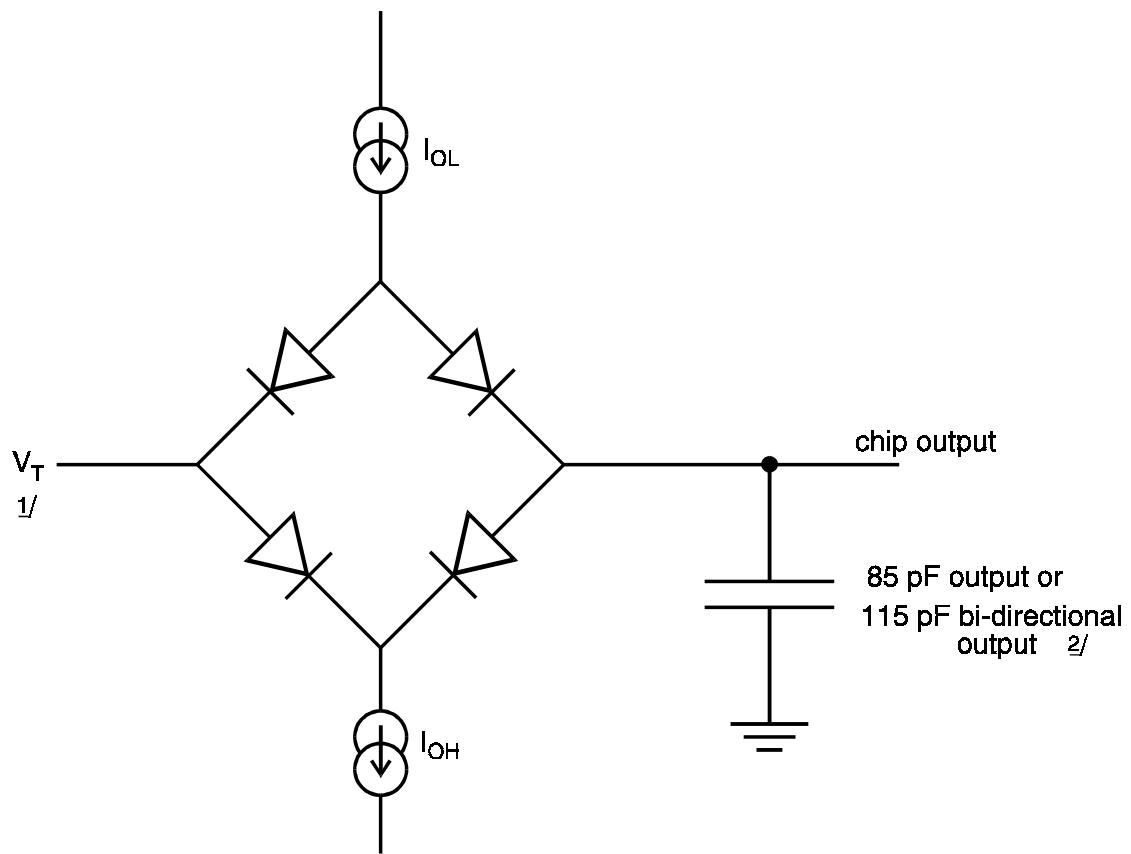


Figure 4-1. Tester Load Circuit

- 1/ V_T is a variable dependent upon the test parameter.
- 2/ This capacitance is actually partially distributed through the fixturing so that the device is actually loaded by a transmission line.

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SHEET 23			REV. C SHEET 23

4.6 Burn-In

4.6.1 Static Burn-In

The Static Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7.

4.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7. Input stimuli (STIM) to exercise the device shall be applied by using the RIGEL Stuck-at Fault test vectors, or a subset thereof, as determined by JPL. At least one output (MON) shall be monitored during burn-in to assure that the output is toggled and the circuit functioning.

4.6.3 Burn-In Conditions

	Static I	Static II	Dynamic	QCI - Life Test
Duration	48 hours	48 hours	240 hours	2000 hours
Voltage	6.5 V	6.5 V	6.5 V	6.0 V
+ Tolerance	+0.1V	+0.1V	+0.1V *	+0.1V *
- Tolerance	-0.25V	-0.25V	-0.25V	-0.25V
Temperature	125 °C	125 °C	125 °C	125 °C
+ Tolerance	+5 °C	+5 °C	+5 °C	+5 °C
- Tolerance	-0 °C	-0 °C	-0 °C	-0 °C

Table 4-6. Burn-In Conditions

* Applies to Average Power Supply Voltage. Tolerance for Dynamic Switching Noise is +0.25V.

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SHEET 24			SHEET 24	

4.6.4 Burn-In Configuration

Pin Name	Pin No. ²²	Type ²³	Burn-In Test Connection ²⁴			Description
			Static I	Static II	Dynamic	
A(7:0)	174-176, 185-187, 189, 190	IN	GND	VDD	VDD	ISB Address Bus (256W).
DP	120	BI6	GND	VDD	VDD	ISB Data Parity.
D(15:0)	124, 126, 132, 134, 136, 138, 140, 145, 147, 151, 153, 155, 159, 161, 163, 165	BI6	GND	VDD	VDD	ISB Data Bus.
DPEn	143	OUT6	GND	VDD	VDD	ISB Data Parity Error.
AREn	122	OUT6	GND	VDD	VDD	ISB Address Range Error.
ADVn	118	IN	GND	VDD	VDD	ISB Address Valid.
RDIR	114	IN	GND	VDD	VDD	ISB Read Direction
DTACKn	105	OUT6	GND	VDD	VDD	ISB Data Transfer Acknowledge
RSDL_INTn	116	OUT6	GND	VDD	VDD	RSDL Interrupt line
M11.9_CLK	77	INPD	GND	VDD	VDD	11.9448MHZ clock
RDECODE	84	IN	GND	VDD	VDD	Select Local Register
PORn	73	IN	GND	VDD	VDD	Power On Reset
SWRST0n	80	IN	GND	VDD	VDD	Software Reset 0
RSA(12:0)	14, 16, 26, 27, 29, 31, 32, 35, 36, 38, 40, 41, 48	OUT6	GND	VDD	VDD	RS Memory Buffer Address Bus
RSD(15:0)	4, 6, 8, 11, 13, 18, 20, 24, 50, 53, 55, 58, 60, 62, 69, 71	BI6	GND	VDD	VDD	RS Memory Buffer Data Bus
RSCSn	33	OUT6	GND	VDD	VDD	RS Memory Buffer Chip Select
RSWEn	46	OUT6	GND	VDD	VDD	RS Memory Buffer Write Enable
RSOEn	43	OUT6	GND	VDD	VDD	RS Memory Buffer Output Enable
DLA_DATA	240	OUT6	GND	VDD	VDD	Downlink Data to TCU A
DLA_X6	239	OUT6	GND	VDD	VDD	Six times Downlink Data Rate Clock to TCU A
DLB_DATA	237	OUT6	GND	VDD	VDD	Downlink Data to TCU B

Table 4-7. Burn-In Configuration

²² The pin numbers of bus signals are in the same sequence as the signals.

²³ For a description of the signal type refer to Table 4-9.

²⁴ All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

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SHEET 25			SHEET 25	

Pin Name	Pin No. ²⁵	Type ²⁶	Burn-In Test Connection ²⁷			Description
			Static I	Static II	Dynamic	
DLB_X6	236	OUT6	GND	VDD	VDD	Six times Downlink Data Rate Clock to TCU B
T0_DATA	234	TRIOD6	GND	VDD	VDD	Downlink Data to T0
T0_DATAn	233	TRIOD6	GND	VDD	VDD	Downlink Data in reverse polarity to T0
T0_X1	231	TRIOD6	GND	VDD	VDD	Downlink Data Rate Clock to T0
T0_X1n	230	TRIOD6	GND	VDD	VDD	Downlink Data Rate Clock in reverse polarity to T0
LV_DATA	245	OUT6	GND	VDD	VDD	Downlink Data to LV
LV_DATAn	246	OUT6	GND	VDD	VDD	Downlink Data in reverse polarity to LV
LV_X1	243	OUT6	GND	VDD	VDD	Downlink Data Rate Clock to LV
LV_X1n	242	OUT6	GND	VDD	VDD	Downlink Data Rate Clock in reverse polarity to LV
BUFSEL	173	OUT6	GND	VDD	VDD	Buffer Select for the DL buffer
BUFSWAP	183	OUT6	GND	VDD	VDD	Swap the DL buffer
EOB	167	IN	GND	VDD	VDD	End of the DL buffer
RSTn	171	OUT6	GND	VDD	VDD	Synchronous Reset
DLREQn	168	OUT6	GND	VDD	VDD	DL request for memory read
DLDONEn	169	IN	GND	VDD	VDD	DL request has been served
DLDATA(15:0)	179-181, 196, 197, 199, 200, 202, 203, 205, 206, 208, 209, 211, 213, 214	IN	GND	VDD	VDD	DL Data bus
PRIME	100	IN	GND	VDD	VDD	Primary string
RSHEALTH	101	IN	GND	VDD	VDD	Redundant String Health
GNDUE	111	IN	GND	VDD	VDD	Ground Update Enabled
XRTIn	112	IN	GND	VDD	VDD	Cross-strapped RTI
RTIn	103	OUT6	GND	VDD	VDD	Real Time Interrupt
ARTIn	109	OUT6	GND	VDD	VDD	ARTIn occurs 5ms before RTI
EFCn	90	OUT6	GND	VDD	VDD	64.005 Hz clock
DEADP	96	OUT6	GND	VDD	VDD	Dead Period

Table 4-7. Burn-In Configuration (Cont'd)

²⁵ The pin numbers of bus signals are in the same sequence as the signals.

²⁶ For a description of the signal type refer to Table 4-9.

²⁷ All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

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SHEET 26			SHEET 26			

Pin Name	Pin No. ²⁸	Type ²⁹	Burn-In Test Connection ³⁰			Description
			Static I	Static II	Dynamic	
RELAYP	98	OUT6	GND	VDD	VDD	2048.148 Hz clock
SE_DP	228	TRIOD6	GND	VDD	VDD	DEADP sent to SE
SE_DPN	227	TRIOD6	GND	VDD	VDD	DEADPN to SE
SE_RTI	225	TRIOD6	GND	VDD	VDD	RTI to SE
SE_RTIn	224	TRIOD6	GND	VDD	VDD	RTIn to SE
BR3n	249	IN	GND	VDD	VDD	ISB Bus Request 3
BR2n	252	IN	GND	VDD	VDD	ISB Bus Request 2
BR1n	93	IN	GND	VDD	VDD	ISB Bus Request 1
BR0n	254	IN	GND	VDD	VDD	ISB Bus Request 0
BG3n	248	OUT6	GND	VDD	VDD	ISB Bus Grant 3
BG2n	250	OUT6	GND	VDD	VDD	ISB Bus Grant 2
BG1n	92	OUT6	GND	VDD	VDD	ISB Bus Grant 1
BG0n	253	OUT6	GND	VDD	VDD	ISB Bus Grant 0
BGABTn	115	OUT6	GND	VDD	VDD	Bus Grant Abort
HOG	94	IN	GND	VDD	VDD	Grant ISB to XBA and EFC.
EX_MSEL	82	IN	GND	VDD	VDD	External Memory Select
EX_RSEL	83	IN	GND	VDD	VDD	External Register Select
EN_DTACKn	107	OUT6	GND	VDD	VDD	Enable DTACKn
ISB1DDIR	75	OUT6	GND	VDD	VDD	ISB Data Bus Direction
XBA_ADENn	86	OUT6	GND	VDD	VDD	XBA Address Enable
XBA_ADDIR	88	OUT6	GND	VDD	VDD	XBA Address bus Direction.
Rigel	220	INPD	GND	VDD	STIM ³¹	Rigel test command.
TCK	217	INPD	GND	VDD	STIM ³¹	Test Circuitry Clock.
TDI	221	INPU	GND	VDD	STIM ³¹	Test Data In.
TMS	222	INPU	GND	VDD	STIM ³¹	Test Mode Select
TRSTn	216	INPU	GND	VDD	STIM ³¹	Test Reset
TDO	218	TRI6	GND	VDD	MON ³²	Test Output Data
PWR	1, 65, 129, 193	VDD	6.5V	6.5V	6.5V (6V for Lifetest)	Vdd Power Pads.
GND	2, 63, 64, 66, 127, 128, 130, 191, 192, 194, 255, 256	VSS	0.0V	0.0V	0.0V	Vss Power Pads.

Table 4-7. Burn-In Configuration (Cont'd)

²⁸ The pin numbers of bus signals are in the same sequence as the signals.

²⁹ For a description of the signal type refer to Table 4-9.

³⁰ All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

³¹ Stimulated Input

³² Monitored Output

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SHEET 27			SHEET 27	

4.6.5 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I _{DDSB}	Static Supply Current		800	µA	80	µA
I _{IL1}	Input Leakage Current Low	-10	10	µA	±1	µA
I _{IL2}	Input Leakage Current Low, Pull-Ups	-550	-50	µA	±55	µA
I _{IL3}	Input Leakage Current Low, Pull-Downs	-10	10	µA	±1	µA
I _{IH1}	Input Leakage Current High	-10	10	µA	±1	µA
I _{IH2}	Input Leakage Current High, Pull-Ups	-10	10	µA	±1	µA
I _{IH3}	Input Leakage Current High, Pull-Downs	50	550	µA	±55	µA
I _{OZL}	Output Leakage Current Low	-10	10	µA	±1	µA
I _{OZH}	Output Leakage Current High	-10	10	µA	±1	µA
I _{OL}	Output Current Low		6	mA	±600	µA
I _{OH}	Output Current High	-6		mA	±600	µA

Table 4-8. Delta Limits

4.7 Pin Type Description

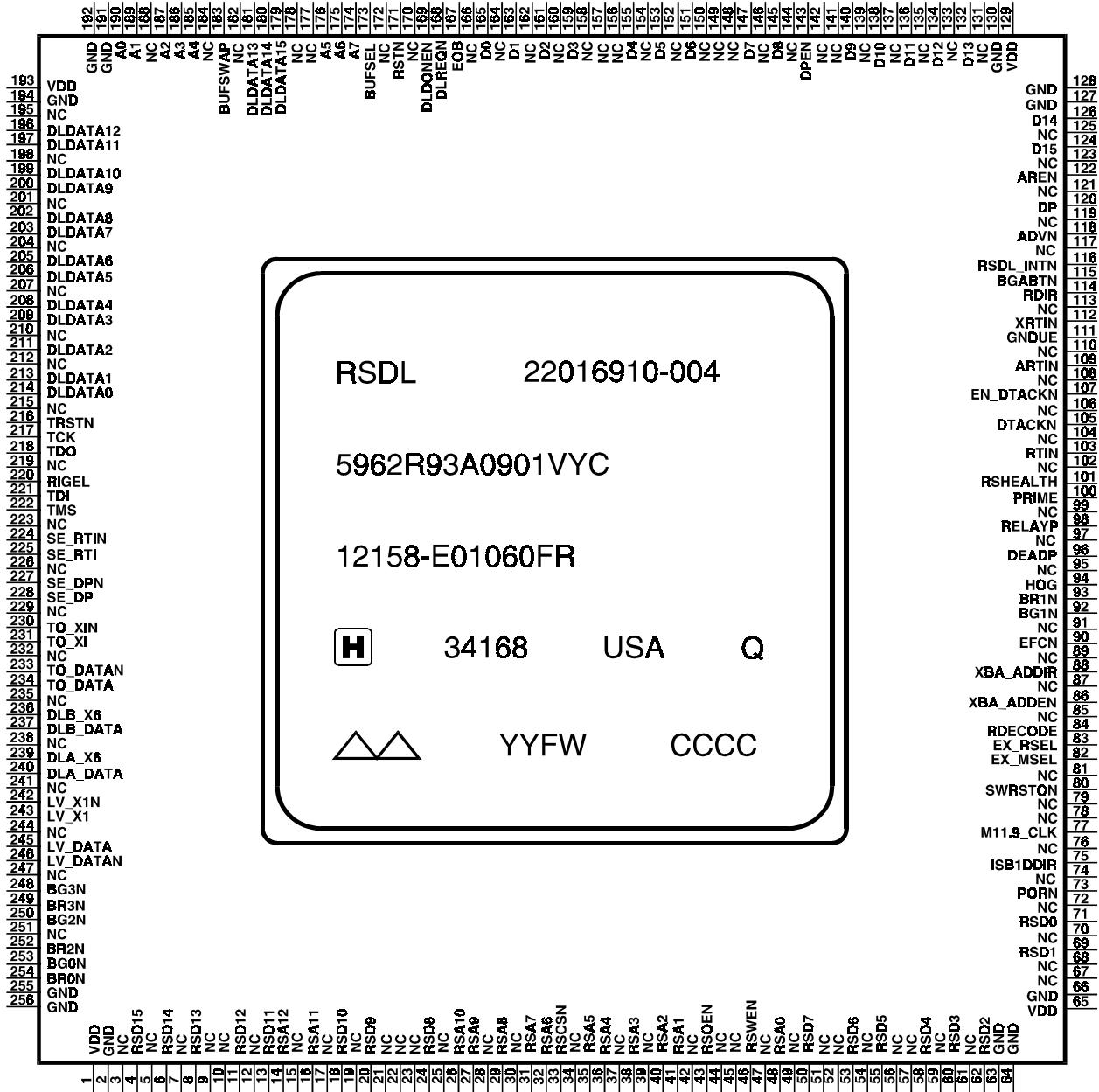
Pin Name	Drive	I/O	Type
IN	=	CMOS,	Input Signal
INPU	=	CMOS,	Input Signal with Pull-up
INPD	=	CMOS,	Input Signal with Pull-down
TRI6	= 6mA,	CMOS,	Tri-State Signal
TRIOD6	= 6mA,	CMOS,	Tri-State Signal, Open Drain
OUT6	= 6mA,	CMOS,	Output Signal
BI6	= 6mA,	CMOS,	Bidirectional Signal

Table 4-9. Pin Type Description

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ST 12158	REV. C	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, REED SOLOMON DOWN LINK (RSDL)	ST 12158	REV. C
SHEET 28			SHEET 28	

5. PHYSICAL CHARACTERISTICS

5.1 Pin Assignment.



5.2 Bonding Diagram

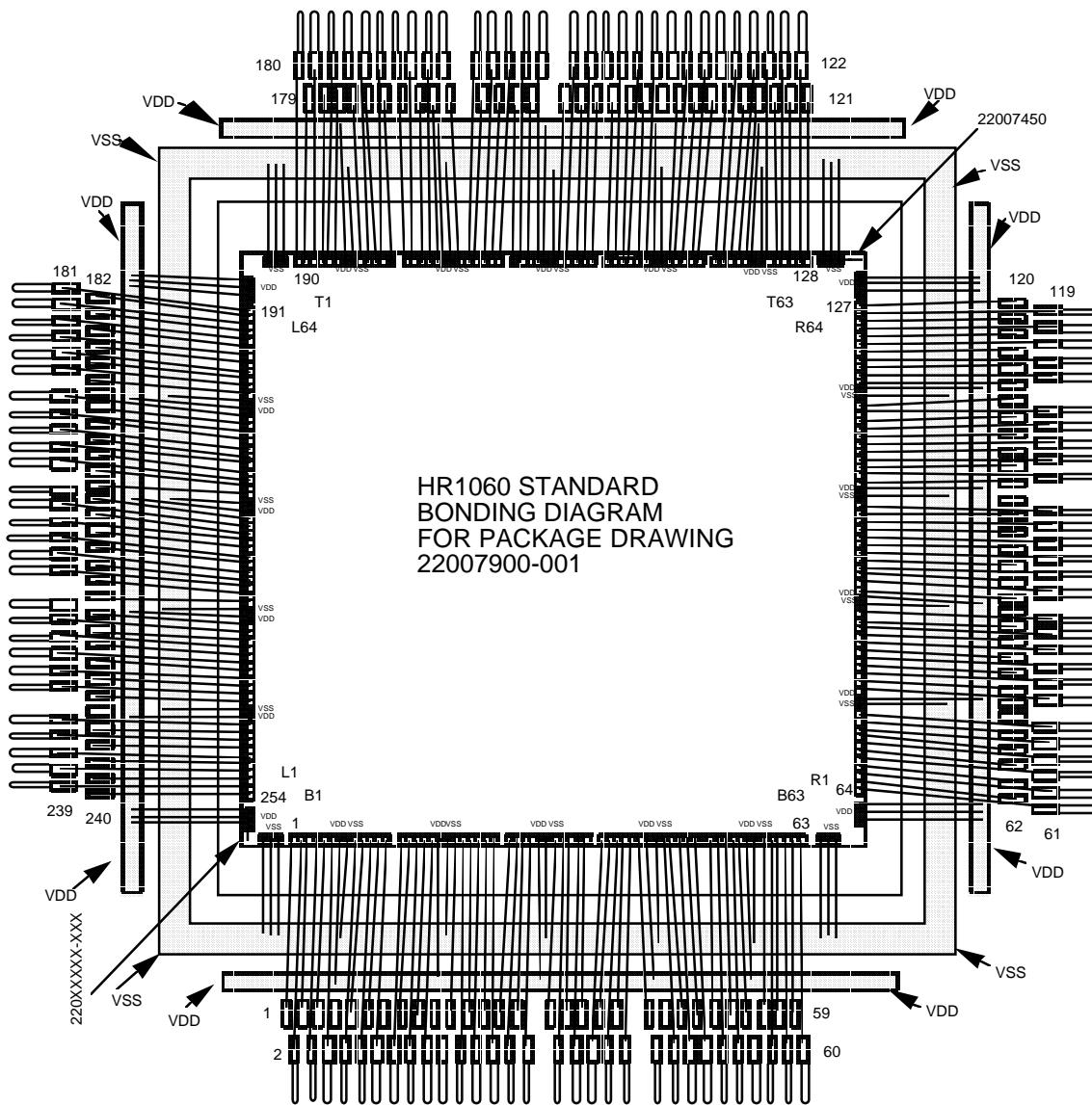
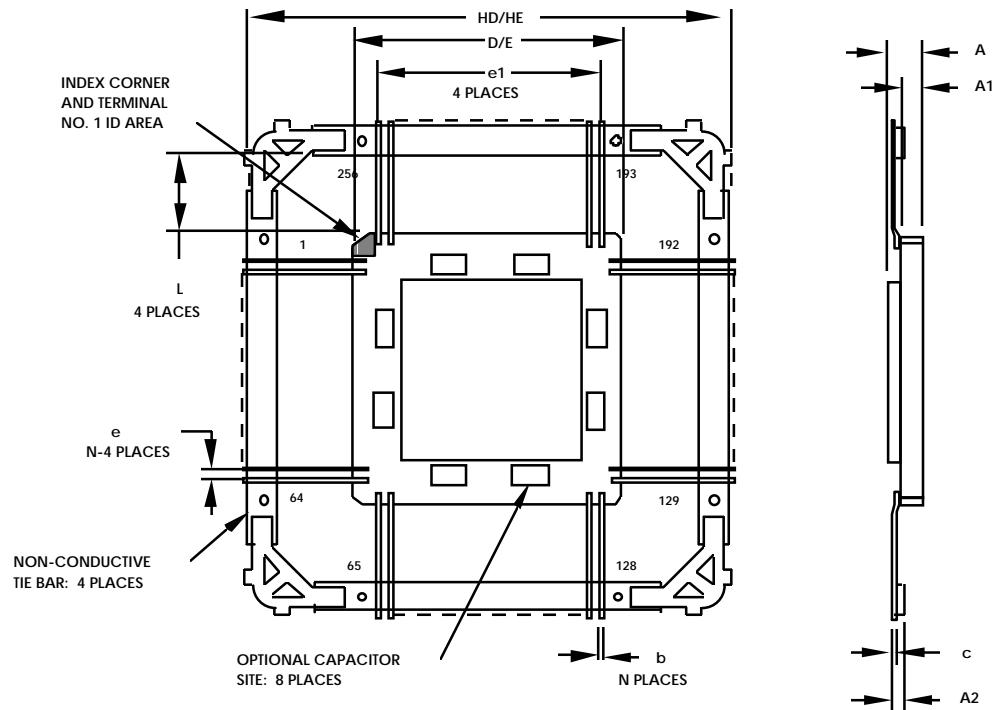


Figure 5-2. Bonding Diagram (256 pin Flatpack)

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12158	REV. C	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, REED SOLOMON DOWN LINK (RSDL)	ST 12158
SHEET 30		REV. C	
		SHEET 30	

5.3 Package Outline.

256 Lead Flat Package



PACKAGE DIMENSIONS		
Symbol	Dimensions in inches	
	min	max
A	0.130	0.160
A1	-	0.130
A2	0.024	0.040
b	0.005	0.009
c	0.004	0.008
D/E	1.445	1.455
e	0.020 BSC	
e1	1.260 BSC	
HD/HE	2.365	2.395
L	0.325	-
N	256	

Figure 5-3. Package Outline (256 pin Flatpack)

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12158	REV. C	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, REED SOLOMON DOWN LINK (RSDL)	ST 12158
SHEET 31			REV. C SHEET 31

5.4 Marking Diagram

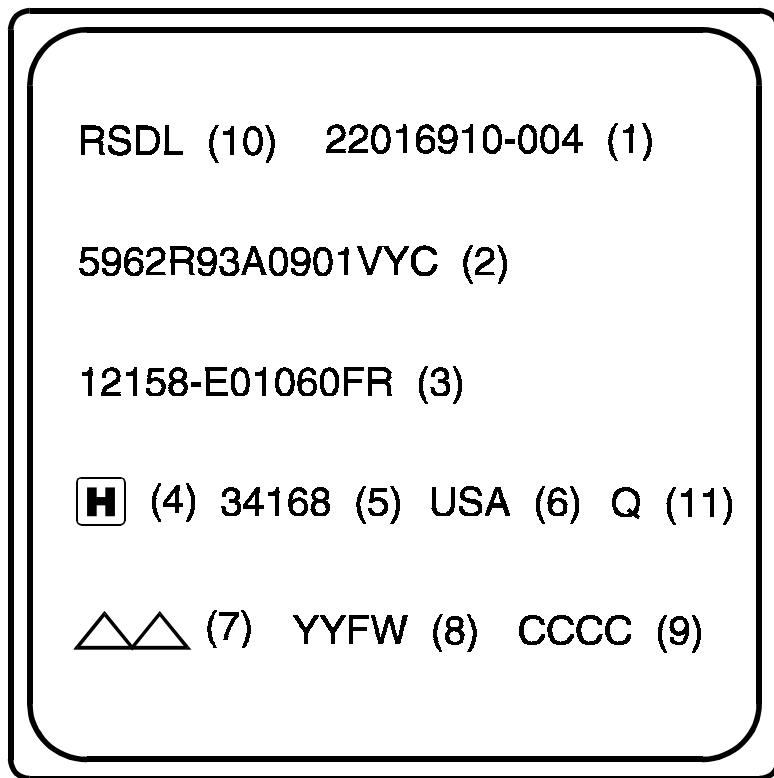


Figure 5-4. Marking Diagram

- (1) Honeywell Part Number
- (2) QML Number (Flight Units only)
- (3) Customer Part Number
- (4) Honeywell Trademark
- (5) Federal Supplier Manufacturing Number
- (6) Country of Origin
- (7) Pin 1 indicator and ESD identifier
- (8) Date Code -Year and Fiscal Week of Lid Seal.
YY = Year
FW = Fiscal Week
- (9) Serialization (Traceability Capability to Die)
- (10) Chip Name (If required)
- (11) QML Mark (Flight Units only)

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ST 12158	REV. C	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, REED SOLOMON DOWN LINK (RSDL)	ST 12158
SHEET 32		REV. C	
SHEET 32			

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Keywords:
Comments:
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Last Saved On: 12/22/94 3:47 PM
Last Saved By: Hubert Schafzahl
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Last Printed On: 08/08/95 2:29 PM
As of Last Complete Printing
Number of Pages: 32
Number of Words: 5,590 (approx.)
Number of Characters: 31,863 (approx.)